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(54) **Determining optimal bias voltages in amplifying circuit**

(57) In an amplifying circuit (10), an amplifier (11) has an input, an output and a direct current supply. A current sensing arrangement measures direct current supplied to the amplifier, and provides a signal, representative of the direct current supplied, to an analog-to-digital converter (38) coupled to the processor (40). The processor outputs a bias voltage control signal from a digital-to-analog converter (42) to control the bias voltage at the input (24) of the amplifier. A factory or field system for a radio is disclosed in which the current supplied to the radio is externally monitored and the information supplied to the radio where internal processing determines the bias level.

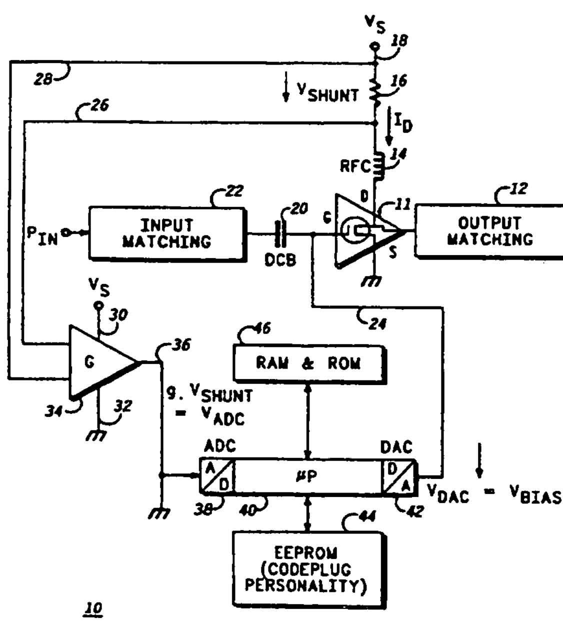

FIG. 1

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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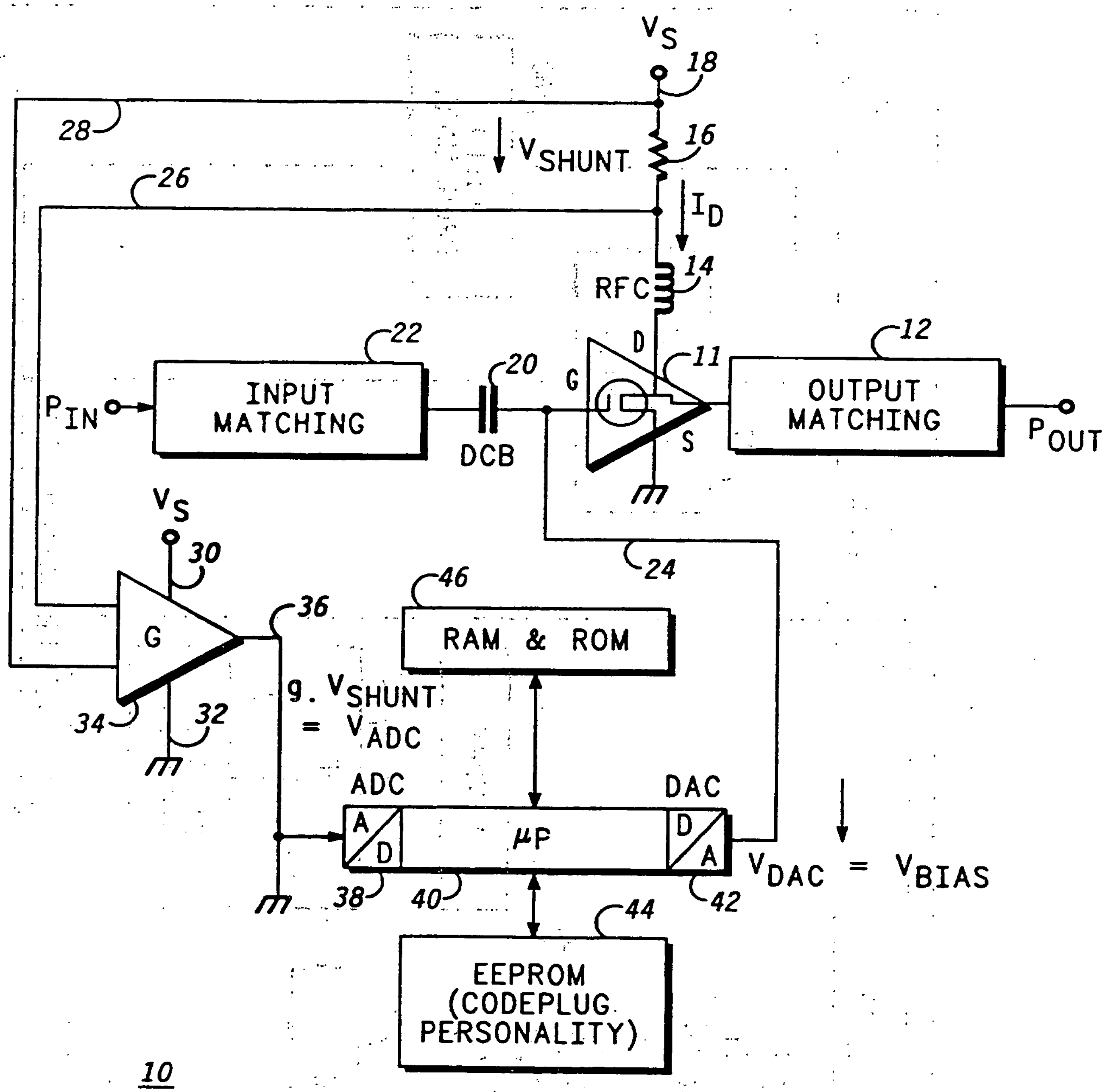

VS
18
28
16
VSHUNT
26
ID
14
RFC
22
12
20
D
11
G
INPUT MATCHING
OUTPUT MATCHING
PIN
POUT
DCB
S
VS
30
24
46
36
RAM & ROM
G
g. VSHUNT = VADC
34
32
ADC
DAC
A
D
μP
D
A
VDAC = VBIAS
38
40
42
44
EEPROM (CODEPLUG PERSONALITY)
10

FIG. 1

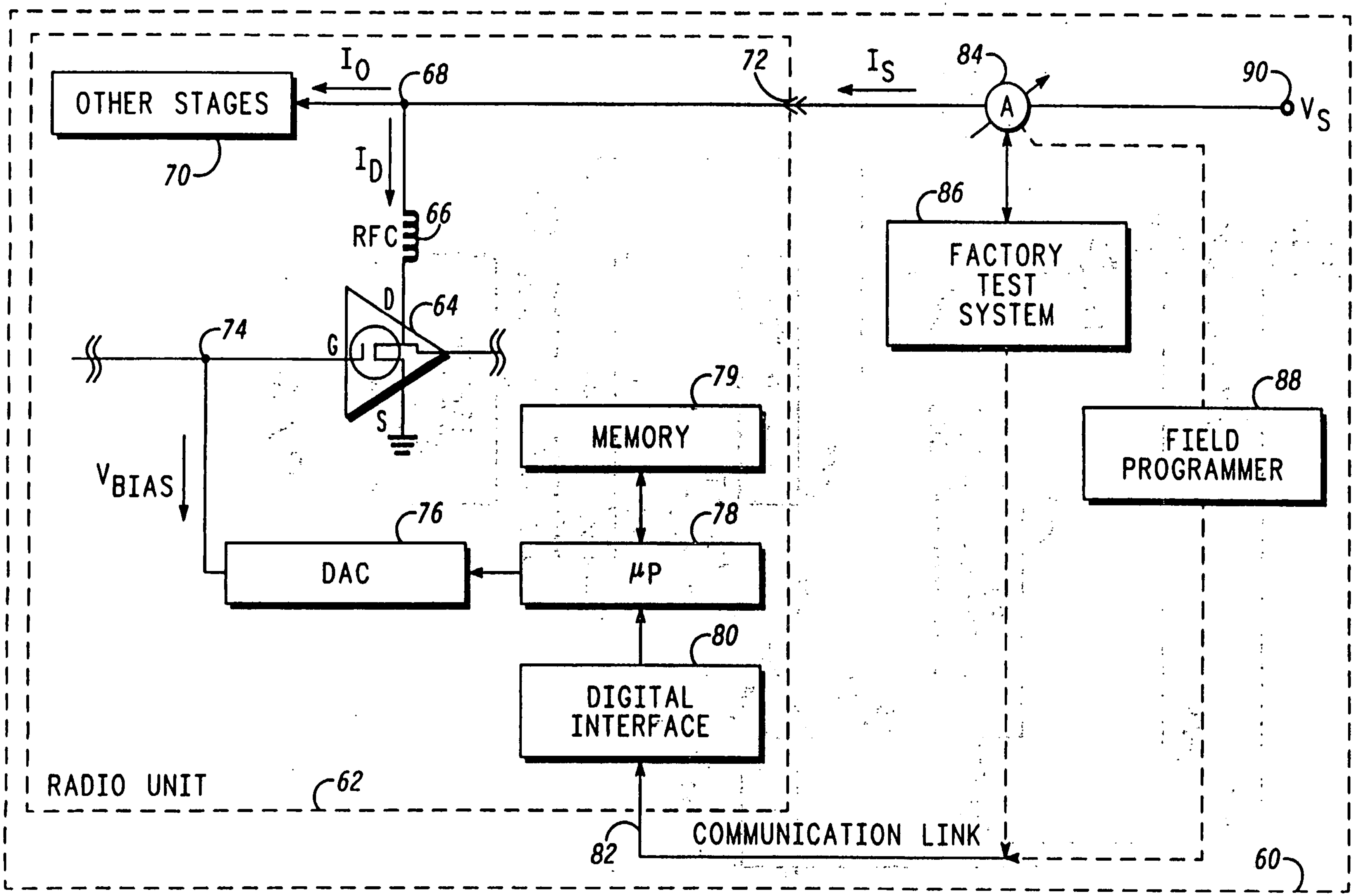
OTHER STAGES
70
I_O
68
I_D
RFC
66
D
64
G
S
74
V_{BIAS}
DAC
76
MEMORY
79
μP
78
DIGITAL INTERFACE
80
RADIO UNIT
62
72
I_S
84
A
90
V_S
86
FACTORY TEST SYSTEM
88
FIELD PROGRAMMER
COMMUNICATION LINK
82
60

FIG. 2

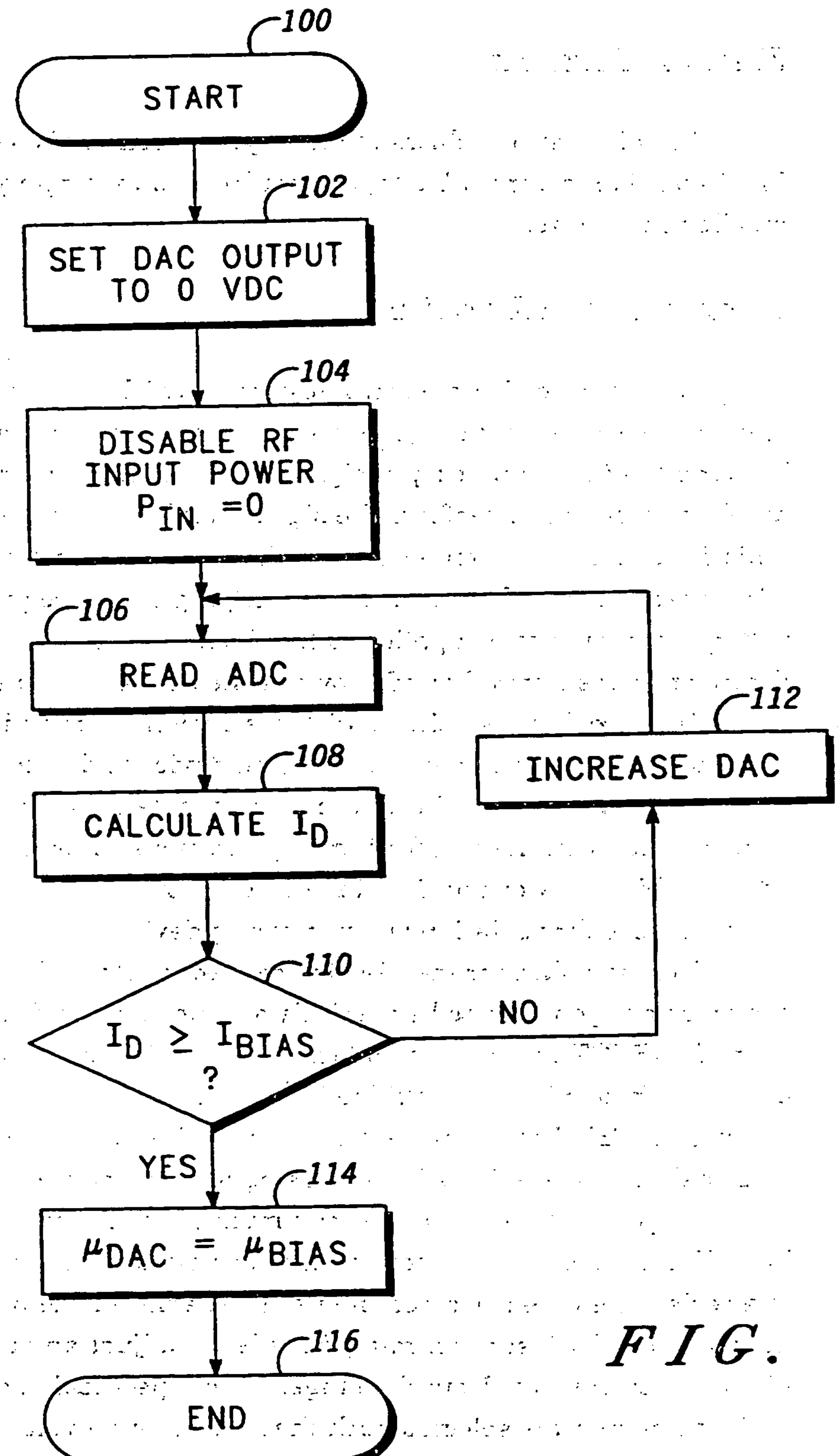
100
START
102
SET DAC OUTPUT TO 0 VDC
104
DISABLE RF INPUT POWER P_{IN} =0
106
READ ADC
108
CALCULATE I_D
110
$I_D \geq I_{BIAS}$?
NO
112
INCREASE DAC
YES
114
$\mu_{DAC} = \mu_{BIAS}$
116
END

FIG. 3

2301248

AMPLIFYING CIRCUIT AND METHOD FOR DETERMINING OPTIMAL BIAS VOLTAGES THEREIN

Field of the Invention

This invention relates to amplifying circuits of electronic equipment. The invention is applicable to, but not limited to, amplifying circuits of mobile radio units.

Background of the Invention

An amplifier is an electronic circuit which accepts an electrical input and provides an electrical output such that there is a prescribed relationship between the input and output signal's. The amplifier circuit requires an amplifying device to perform the signal amplification operation. For the majority of amplification devices, such as bipolar junction transistors, field-effect transistors (FETs) etc., the amplifying device requires specific bias voltages/currents to be applied to the device terminals' to ensure that the device operates correctly and provides the desired output signal.

One problem associated with the design of amplifier circuits is that the desired bias voltage/current varies from device to device, especially between different production batches, even when the devices are to be used for the same application. Hence, for some applications, there is a need for an adaptive bias network design, instead of a fixed bias network design, to accommodate for variations in amplifying device characteristics.

In particular, for metal-oxide semiconductor (MOS)FET applications, the bias voltage needs to be precisely arranged around the threshold voltage of the MOSFET device, to avoid excessive drain current consumption of the device, as known to those skilled in the art. There are several methods of biasing MOSFETs to achieve very precise bias voltages on the MOSFET gate terminal. These methods involve using a fixed voltage reference, arranged to be at a higher voltage than the maximum possible threshold voltage of the MOSFET device, and a potential divider network. Currently, the resistance of a resistive element located in one of the arms of the potential divider is adjusted, e.g. by laser trimming, in order to adjust an output of the potential divider network to a desired voltage. More specifically, a value of the resistive element is selected such that it delivers a voltage that is below the lowest possible threshold voltage of the amplifying device prior to any trimming. Clearly, as the resistive element is trimmed, its resistance,

together with the voltage across the resistive element, increases. The trimming process is complete when the gate bias voltage has reached a desired voltage level, with the optimal bias point being determined by measuring the drain current of the amplifying device. The accuracy in setting the gate bias voltage is dictated by the accuracy of the trimming process.

A problem associated with using a laser trimming process is "overshoot", which results in excessive trimming of the resistive element and hence, a non-optimal gate bias voltage setting. Laser trimming stations are also very expensive and hence, are not usable in 'the field' for repairing or replacing amplifier devices and circuits. Consequently board swapping or radio unit exchanging is currently a more expedient solution for the repair of a faulty amplification circuit.

Thus, it is desirable to have an accurately biased amplifying circuit with a method of optimally setting the gate bias voltage. It would also be beneficial to have an arrangement for re-optimising the gate bias voltage settings in 'the field', to allow for remote fitting of replacement amplifier devices having different operational characteristics.

Summary of the Invention

In a first aspect of the present invention, an amplifying circuit is provided comprising an amplifying device having an input, an output and a direct current supply for providing direct current to the amplifying device. The amplifying circuit further comprises a bias voltage connection for setting a bias voltage at the input of the amplifying device and a current sensing means for measuring the direct current supplied to the amplifying device and for providing a first signal representative of the supplied direct current. The amplifying circuit further comprises an analog-to-digital converter which is operably coupled to the current sensing means for digitizing the first signal, output from the current sensing means, to provide a digitized first signal. A processing device is included which is operably coupled to the analog-to-digital converter for processing the digitized first signal and for providing a digital bias voltage control signal to a digital-to-analog converter. The digital bias voltage control signal is converted to an analog bias voltage control signal by the digital-to-analog converter to adjust the bias voltage at the input to the amplifying device. Preferably the processing device is coupled to

a memory element for storing the bias voltages and corresponding direct current supply levels.

In this manner, an optimal bias voltage of the amplifying device is advantageously controlled according to the direct current supplied to the amplifying device.

Preferably the current sensing means comprises a shunt resistor, operably coupled to the direct current supply of the amplifying device for providing a signal representative of the direct current supplied to the amplifying device, and a direct current amplifier for providing an amplified direct current level signal to the analog-to-digital converter. The direct current supplied to the amplifying device is calculated by dividing the voltage signal, measured at the input to the analog-to-digital converter, by a resistive calibration factor. The resistive calibration factor is equal to the value of the shunt resistance in the current sensing means multiplied by the voltage gain of the direct current amplifier.

In this manner, the level of direct current supplied to the amplifying device is easily determined from the first signal input to the analog-to-digital converter.

In a second aspect of the present invention, an amplifying circuit is provided comprising a field-effect transistor having an input, an output, a direct current supply for providing direct current to the field-effect transistor, and a bias voltage control input for controlling a bias voltage at the input of the field-effect transistor. The amplifying circuit further comprises a processing device for processing operational information of the field-effect transistor and for providing a bias voltage control signal. A digital-to-analog converter is also provided, operably coupled to the bias voltage control input of the field-effect transistor, for converting the digital bias voltage control signal to an analog bias voltage control signal to adjust the bias voltage at the input to the field-effect transistor.

In this manner, the bias voltage input to the field-effect transistor is adjusted according to the operational information of the field-effect transistor, processed by the processing device.

In a third aspect of the present invention a programming means is provided comprising a radio unit having a processing device for receiving communications from a remote controller and a direct current input for receiving a direct current power source. The programming means further comprises a remote current sensing means operably coupled to the direct

current input of the radio unit for providing a second signal indicative of the direct current supplied to the radio unit, and a remote controller, operably coupled to the processing device of the radio unit and the remote current sensing means, for programming bias voltage information into the processing device of the radio unit dependent upon the level of the second signal.

In this manner, bias voltage information is programmed into the processing device of the radio unit by the remote controller.

Preferably, the processing device is operably coupled to a memory element and the remote controller is either a field programming unit for remotely programming bias voltage information into the memory element or a factory test system for pre-programming bias voltage information into the memory element during manufacture of the radio unit. Advantageously, re-optimisation of the gate bias voltage settings in 'the field' is possible, permitting the remote fitting of replacement amplifier devices.

In a fourth aspect of the present invention, a method of determining optimal bias voltages for an amplifying circuit having an amplifying device is provided. The amplifying device has input and output ports and a direct current supply operably coupled to a current sensing means. The amplifying circuit also includes an analog-to-digital converter, operably coupled to the current sensing means, a microprocessor and a digital-to-analog converter for providing bias voltage control to the input of the amplifying device. The method comprises the steps of measuring the direct current supplied to the amplifying circuit at the current sensing means, providing an indication of the direct current supply to the analog-to-digital converter, and processing the direct current supply information at the processing device. The method further comprises the steps of comparing the direct current supplied to the analog-to-digital converter to the bias voltage output from the digital-to-analog converter, at the microprocessor, and adjusting the digital-to-analog converter output until a required bias voltage is achieved.

In this manner, the known bias voltage input to the amplifying device is compared to the direct current supplied to the amplifying device and adjusted accordingly. Advantageously, an optimal setting for the bias voltage of each and every amplifying device, independent of the varying operational characteristics of the amplifying devices, are obtained.

Preferably the input port to the amplifying device is initially disabled, without removing the bias voltage control. In addition, the direct current supplied to the remainder of the radio unit is subtracted from the total level

of direct current supplied to the radio unit, to determine the level of direct current supplied to the amplifying circuit. In a preferred feature the method further comprises the advantageous step of storing values for bias voltages and the corresponding direct current supply levels into a memory element of the processing device to be retrieved for future internal re-programming of bias voltages of the amplifying circuit.

A preferred embodiment of the invention will now be described, by way of example only, with reference to the drawings.

Brief Description of the Drawings

FIG. 1 is a block diagram of an amplifying circuit according to a preferred embodiment of the first aspect of the invention.

FIG. 2 is a block diagram of a programming means, for programming bias voltage information into a radio unit, according to a preferred embodiment of the second aspect of the invention.

FIG. 3 is a flowchart describing a method for determining optimal bias voltages in accordance with the preferred embodiments of the inventions of FIG. 1 or FIG. 2.

Detailed Description of the Drawings

Referring first to FIG. 1, a block diagram of an amplifying circuit 10 according to a preferred embodiment of the invention is shown. The amplifying circuit 10 comprises an amplifying device 11 e.g. a metal oxide semiconductor field-effect transistor (MOSFET), having drain (D), gate (G) and source (S) terminals. A voltage 18 is supplied to the drain terminal of the amplifying device 11 via a shunt resistor 16 and a radio frequency (RF) choke 14. The drain terminal of the amplifying device 11 is also connected to an output port via an output matching circuit 12. The amplifying device 11 receives an input signal onto its gate terminal via an input matching circuit 22 and a direct current (dc) blocking capacitor 20. Bias voltage is also input to the gate terminal via the bias voltage input 24. The source terminal of the amplifying device 11 is connected to a zero dc voltage point (earth). The supply voltage at the input of the shunt resistor 16 and the voltage at the output of the shunt resistor 16 are connected to the input of a dc amplifier 34 via paths 26 and 28. The dc amplifier 34 has a supply voltage 30 and is

connected to earth via path 32. The dc amplifier output 36 is input to an analog-to-digital converter (ADC) 38, which is operably coupled to a processing device 40, e.g. a microprocessor, and a digital-to-analog converter (DAC) 42. The processing device 40 is connected to a memory unit 46, containing random access memory (RAM) and read only memory (ROM) facilities, and an electronically erasable programmable read only memory (EEPROM) 44, used as a codeplug personality for the processing device 40. The DAC output is operably coupled to the bias voltage input 24 of the amplifying device 11.

In operation, the amplifying device 11 is activated by the application of a supply voltage 18 and the operating mode of the amplifying device 11 is determined by the bias voltage input 24, which sets a bias voltage at the input of the amplifying device 11. A current sensing means comprises the shunt resistor 16, operably coupled to the direct current supply of the amplifying device 11, to provide a first signal representative of the direct current supplied to the amplifying device 11. The current sensing means further comprises the dc amplifier 34 for providing an amplified first signal to the analog-to-digital converter 38. In this manner the current sensing means measures the direct current (drain current (I_D)) supplied to the amplifying device 11. The drain current (I_D) drawn by the amplifying device 11 is proportional to the voltage drop across the shunt resistor 16. This voltage drop is input to the dc amplifier 34, of gain 'g', to provide an input voltage 'V_{ADC}' (first signal) to the analog-to-digital converter (ADC) 38 which is representative of the shunt voltage 'V_{shunt}' multiplied by the gain 'g' of the dc amplifier 34, e.g. $V_{ADC} = g^* V_{shunt}$. The gain 'g' of the dc amplifier 34 is chosen for best operating conditions of the ADC 38. The ADC 38 is operably coupled to the current sensing means for digitizing the first signal from the current sensing means to provide a digitized first signal. The processing device 40 processes the digitized first signal, to determine the drain current drawn by the amplifying device 11, and provides a digital bias voltage control signal to a digital-to-analog converter (DAC) 42. The DAC 42 converts the digital bias voltage control signal to an analog bias voltage control signal which controls the bias voltage at the input of the amplifying device.

The use of such a self-biasing arrangement is based on the capability of the processing device 40 to accurately determine the drain current of the

amplifying device 11, by calibrating the amplifying circuit 10. A resistive calibration factor G is obtained by solving the following equations:

$$I_D = (V_{shunt} / R_{shunt}) \quad [1]$$

where $V_{shunt} = V_{ADC} / g$

If the calibration factor G is defined as:

$$G = R_{shunt} * g \quad [2]$$

$$I_D = V_{ADC} / G \quad [3]$$

Advantageously the bias voltage of the amplifying device 11 is continuously optimised according to the operating mode of the amplifying circuit 10. This continuous optimisation is accomplished, at the processing device 40, by dividing the voltage input to the ADC 38 (V_{ADC}) by the pre-calculated calibration factor (G) to obtain the drain current (I_D) for a particular operating mode. The self-biasing process needs only to be performed once during the manufacturing process or alternatively in the 'field' should a defective amplifying device 11 be replaced.

Referring now to FIG. 2, a block diagram of a programming means 60 for programming bias voltage information into a radio unit 62, according to a preferred embodiment of the invention is shown. A programming means 60 comprises a radio unit 62, operably coupled via a communication link 82 to a remote controller. The remote controller is either a factory test system 86 or a field programmer 88. The remote controller is operably coupled to an remote current sensing means, e.g. an ammeter 84, connected in the voltage supply line 90 to the radio unit 62. The radio unit 62 comprises an amplifying circuit, supplied by a drain current I_D, together with other radio stages supplied by a supply current I_o. The total current supplied to the radio unit 62, I_{supply}, is input to a current splitter 68 which divides I_{supply} into I_o and I_D. The radio unit 62 is provided with a dc supply via the battery connector 72. The amplifying circuit comprises an amplifying device 64 e.g. a metal oxide semiconductor field-effect transistor (MOSFET), having three terminals, drain (D), gate (G) and source (S). The drain current is applied to the drain terminal of the amplifying device 64 via a RF choke 66. The drain terminal, D, and the gate terminal, G, of the amplifying device are also connected to additional input and output circuits within the amplifying circuit. Bias voltage is input to the gate terminal via the bias voltage input 74. The bias voltage is supplied from a digital-to-analog converter (DAC) 76,

which is operably coupled to a processing device 78, e.g. a microprocessor. The processing device 78 is connected to memory elements 79 and a digital interface 80, which is operably coupled to the remote controller via the communication link 82.

In operation, the remote current sensing means, e.g. an ammeter 84, registers the direct current supplied to the radio unit 62. The ammeter 84 is operably coupled to the direct current input of the radio unit 62 for providing a second signal indicative of the direct current supplied to the radio unit 62. The supplied direct current is a combination of the drain current I_D supplied to the amplifying device 64 and the current supplied to the other stages 70 of the radio unit I_o. Hence, if I_o is known, the drain current I_D, for a particular mode of operation of the radio unit 62, is determined from a reading on the ammeter 84. The remote controller, i.e. the factory test system 86 or the field programmer 88, is operably coupled to the processing device 78 of the radio unit 62 and the remote current sensing means. The remote controller programs bias voltage information into the processing device 78 of the radio unit 62 dependent upon the level of the second signal.

In this manner, and advantageously, the bias voltage of the amplifying device 64 is optimally programmed in the field for the different operating modes of the amplifying circuit. Hence, should a defective amplifying device 64 be replaced, the amplifying circuit is re-programmed to operate optimally for the particular characteristics of the new amplifying device.

Preferably, the processing device 78 of the radio unit 62 is operably coupled to a memory element 79 and the remote controller is either a field programming unit 88, for remotely programming bias voltage information into the memory element 79, or a factory test system 86 for pre-programming bias voltage information into the memory element 79 during manufacture of the radio unit 62. In a preferred embodiment of the invention, the memory element also stores optimal bias voltages for different temperatures of the amplifying device 64 and operating frequencies of the radio unit 62 in addition to the drain current I_D information.

A method for determining optimal bias voltages for an amplifying circuit is provided which can be implemented in conjunction with either of the preferred embodiments of the invention described above in each of which the amplifying circuit has an amplifying device with input and output ports, a direct current supply to the amplifying device which is operably coupled to a current sensing means, an analog-to-digital converter operably coupled to

the current sensing means, a processing device and a digital-to-analog converter for providing a bias voltage to the amplifying device. The method comprises the steps of measuring the direct current supplied to the amplifying circuit by the current sensing means and providing a third signal, indicative of the direct current supplied to the amplifying circuit, to the analog-to-digital converter. Preferably, in order to measure the direct current supplied to the amplifying device the input port to the amplifying device is disabled, to remove the effects of any input radio frequency signals, without removing the bias voltage. The direct current supplied to the amplifying circuit is determined by subtracting the direct current supplied to other stages of the radio unit from the direct current supplied to the radio unit. The third signal is processed at the processing device to determine the direct current supplied to the amplifying device. The direct current supplied to the amplifying device is then compared to a bias voltage output from the digital-to-analog converter and the bias voltage output from the DAC adjusted by the processing device until a required bias voltage is reached. In addition, the bias voltages are preferably stored with corresponding levels of direct current supplied to the amplifying device into a memory element which is operably coupled to the processing device for future re-programming of bias voltages of the amplifying device.

Referring now to FIG. 3, a flowchart describing the method for determining optimal bias voltages for an amplifying circuit, as shown in either of FIGs 1 and 2 for example in the processing device 40 or the processing device 78. The process is initiated when optimal bias voltages are requested as shown in step 100. The digital-to-analog converter output is set to a pre-determined output voltage, i.e. zero volts, as in step 102. Any radio frequency (RF) input to the amplifying circuit is disabled, as in step 104, and the drain current I_D supplied to the amplifying circuit determined from the voltage input to the analogue to digital converter, as shown in step 106 and step 108. If the drain current I_D is less than the required bias current I_{bias}, as in step 110, the bias voltage supplied from the digital-to-analog output is increased, as shown in step 112, and the new drain current I_D determined, as shown in step 106 and step 108. This process continues until the drain current drain current I_D is equal to or greater than the bias current drain current I_{bias}, as in step 110. When the drain current drain current I_D has reached this level the processing device sets the digital-to-analog converter

output to the appropriate voltage, as in step 114, and the process of determining optimal bias voltages is completed, as shown in step 116.

Thus an accurately biased amplifying circuit with a method of optimally setting the gate bias voltage is provided. A programming means 60 is also provided for remotely programming optimal gate bias voltage settings in 'the field'.

Claims

1. An amplifying circuit comprising:

an amplifying device having an input, an output and a direct current supply for providing direct current to the amplifying device,

a bias voltage input for setting a bias voltage at the input of the amplifying device,

current sensing means for measuring the direct current supplied to the amplifying device and providing a first signal representative of the supplied direct current, and

an analog-to-digital converter operably coupled to the current sensing means for digitizing the first signal from the current sensing means to provide a digitized first signal,

a processing device for processing the digitized first signal and providing a digital bias voltage control signal,

a digital-to-analog converter for converting the digital bias voltage control signal to an analog bias voltage control signal to adjust the bias voltage at the input of the amplifying device.

2. An amplifying circuit according to claim 1, wherein the current sensing means comprises:

a shunt resistor operably coupled to the direct current supply of the amplifying device for providing the first signal representative of the direct current supplied to the amplifying device, and

a direct current amplifier for providing an amplified first signal to the analog-to-digital converter.

3. An amplifying circuit according to claim 2, wherein the level of direct current supplied to the amplifying device is calculated by dividing the voltage signal measured at the input to the analog-to-digital converter by a resistive calibration factor, and wherein the resistive calibration factor is equal to the value of the shunt resistance in the current sensing means multiplied by the voltage gain of the direct current amplifier.

4. An amplifying circuit according to any of the preceding claims wherein the processing device is coupled to a memory element for storing bias voltages

and corresponding levels of supplied direct current of the amplifying device.

5. An amplifying circuit comprising:

a field-effect transistor having an input, an output, a direct current supply for providing direct current to the field-effect transistor, and a bias voltage input for setting a bias voltage at the input of the field-effect transistor,

a processing device for processing operational information of the field-effect transistor and providing a bias voltage control signal, and

a digital-to-analog converter operably coupled to the bias voltage input of the field-effect transistor for converting the bias voltage control signal to an analog bias voltage control signal for adjusting the bias voltage input to the field-effect transistor.

6. A programming means comprising:

a radio unit having a processing device for receiving communications from a remote controller and a direct current input for receiving direct current,

a remote current sensing means operably coupled to the direct current input of the radio unit for providing a second signal indicative of the direct current supplied to the radio unit, and

a remote controller operably coupled to the processing device of the radio unit and the remote current sensing means, for programming bias voltage information into the processing device of the radio unit dependent upon the level of the second signal.

7. A programming means according to claim 6, wherein the processing device of the radio unit is operably coupled to a memory element, for storing bias voltage information, and the remote controller is a field programming unit for remotely programming bias voltage information into the memory element.

8. A programming means according to claim 6, wherein the processing device of the radio unit is operably coupled to a memory element, for storing bias voltage information, and the remote controller is a factory test system for pre-programming bias voltage information into the memory element during manufacture of the radio unit.

9. A method of determining optimal bias voltages for an amplifying circuit having an amplifying device with input and output ports, a direct current supply to the amplifying device which is operably coupled to a current sensing means, an analog-to-digital converter operably coupled to the current sensing means, a processing device and a digital-to-analog converter for providing a bias voltage to the amplifying device, the method comprising the steps of:

measuring direct current supplied to the amplifying circuit by the current sensing means,

providing a third signal, indicative of the direct current supplied to the amplifying circuit, to the analog-to-digital converter,

processing the third signal at the processing device to determine the direct current supplied to the amplifying device,

comparing, by the processing device, the direct current supplied to the amplifying device to a bias voltage output from the digital-to-analog converter,

adjusting, by the processing device, the digital-to-analog converter output until a required bias voltage is reached.

10. The method of claim 9, wherein the step of measuring the direct current supplied to the amplifying device from the measured analog-to-digital converter input voltage level, further comprises the steps of:

disabling the input port to the amplifying device without removing the bias voltage, and

subtracting the direct current supplied to other stages of the radio unit, from the direct current supplied to the radio unit, to determine the direct current supplied to the amplifying circuit.

11. The method of claim 9 further comprising the step of storing bias voltages with corresponding levels of direct current supplied to the amplifying device into a memory element operably coupled to the processing device for future re-programming of bias voltages of the amplifying device.

Patents Act 1977
Examiner's report to the Comptroller under Section 17
(The Search report)

14

Application number
GB 9510666.2

Relevant Technical Fields

(i) UK Cl (Ed.N) H3W (WUE, WUS)

(ii) Int Cl (Ed.6) H03F (1/02)

Search Examiner
D MIDGLEY

Date of completion of Search
27 JULY 1995

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE: WPI

Documents considered relevant following a search in respect of Claims :-
1-5, 9-11

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
X	EP 0401013 A2 (NEC) whole document	1, 5, 9 at least

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).